A Lock Detector Circuit for Dejitter Phase Lock Loop (PLL) Applications

Background of the Invention

Field of the Invention

[0001] This invention relates to phase and frequency synchronized oscillatory circuits such as a phase lock loop. More particularly, this invention relates to circuits that detect loss of phase and frequency synchronization of an output timing signal of a phase lock loop with its frequency reference signal and provide an alarm indicative of the loss of synchronization.

Description of Related Art

[0002] In present high frequency digital communication and telecommunications systems, the network terminals must provide timing signals that synchronize with the incoming transport signals to recover the information. An exemplary telecommunication system is the Synchronous Optical Network (SONET). SONET is a standard for optical transport formulated by the Exchange Carriers Standards Association (ECS) for the American National Standards Institute (ANSI). ANSI generally set the standards for telecommunication within the United States.

[0003] SONET as the name implies is a synchronous network thus requiring all terminals on a SONET network to have internal clocking that is traceable to a highly stable reference clocking supply. The reference timing of a network terminal is embedded in the transport signal and the receiver synchronizes its local oscillator to the incoming embedded reference timing signal. Alternately, each terminal maybe connected to a building integrated timing supply (BITS). BITS is a highly accurate oscillator signal transferred independently of the transport signal for each terminal to achieve synchronicity.

[0004] Each terminal has a receiver to receive and buffer the transport signal. The receiver is connected to a clock extraction circuit that extracts the reference timing signal from the transport signal. The clock extraction circuit is connected to a phase lock loop that generates the local timing signal for the terminal. Alternately, the phase lock loop is connected to a BITS clock extractor, which extracts the highly accurate reference timing signal from the BITS communication link.

[0005] Clock extraction from the transport signal is well known in the art as illustrated in U. S. Patent 5,963,608 (Casper et al.). Casper et al. has a data rate estimator that derives an estimate of the data rate of data contained in the digital data signal. A frequency estimator derives an estimate of the frequency of the output of phase lock loop. During an initial frequency acquisition mode, the sweep controller sequentially varies

an analog voltage applied to the voltage controlled oscillator of the phase lock loop, until the estimate of the data rate effectively corresponds to the estimate of the frequency of the output of the voltage controlled oscillator. This terminates the frequency acquisition mode and initiates a phase acquisition mode. A loop filter is swept until the frequency of the phase lock loop equal to the actual frequency of the embedded clock signal, thereby locking the loop to the embedded clock.

[0006] The structure of a phase lock loop is well known in the art as shown in "Phase-Lock Loop-Based (PLL) Clock Driver: A Critical Look at Benefits Versus Costs," Nayan Patel, SCAA033A, Texas Instruments, March 1997, and "Phase-Locked Loops for High-Frequency Receivers and Transmitters – Part 1" Curtin and O'Brien, Analog Dialogue, 33-3, 1999. Refer now to Fig. 1 for a brief review of the structure and operation of the phase lock loop. The key component of the phase lock loop **5** is a voltage controlled oscillator **25**. The voltage controlled oscillator **25** may be crystal controlled oscillator (VCXO) or a surface acoustical wave (SAW) filter controlled oscillator (VCSO). The fundamental frequency of the voltage controlled oscillator as established by the crystal or SAW filter is adjusted or pulled in proportion to an input voltage signal $\mathbf{V_{IN}}$. Thus the frequency of the output timing signal $\mathbf{F_{out}}$ is modified in response to changes in the level of the input voltage signal $\mathbf{V_{IN}}$. The input reference signal $\mathbf{F_{ref}}$ is the timing reference signal either embedded in the transport signal or provided by the BITS. The phase-frequency detector **10** receives the input

reference signal F_{ref} and a fedback form of the output timing signal F_{out}. The input reference signal F_{ref} and the fedback form of the output timing signal F_{out} are compared to determine the phase and frequency equivalence of the input reference signal F_{ref} and the fedback form of the output timing signal F_{out}. The phase-frequency detector **10** has an output **UP** indicating that the phase-frequency of the voltage control oscillator **25** needs to be adjusted to increase the frequency of the output timing signal F_{out}. The second output **DOWN** of the phase-frequency detector **10** indicated that the voltage controlled oscillator **25** needs to be adjusted to decrease the frequency of the output timing signal F_{out}. The output signal **UP** and **DOWN** of the phase-frequency detector **10** are the inputs to the charge pump **15**. The charge pump **15** provides an output current I_{CP} that is proportional to the desired frequency of the output timing signal F_{out}. The output current I_{CP} is transferred to the low pass filter **20**. The low pass filter **20** removes any undesired high frequency noise components that may be generated in the phase-frequency detector **15** or the charge pump **20** and creates the input adjustment voltage V_{in} for the voltage controlled oscillator **25**.

[0007] As is known in the art the frequency of the input reference signal F_{ref} may be a submultiple of the frequency of the output timing signal F_{out}. If this is the case for the design of the phase lock loop as illustrated, the frequency divider **30** is optionally placed in the feedback path of the output timing signal F_{out}. The frequency divider divides the frequency of the

output timing signal F_{out} such that the input reference signal F_{ref} is compared with a feedback signal that is a submultiple of the output timing signal F_{out}.

[0008] In digital phase lock loops the outputs **UP** and **DOWN** of the phase-frequency detector **10** are generally digital signals as shown in Fig. 2. In this example the phase frequency detector **10** determines phase and frequency synchronicity at the fall **30**, **35**, and **40** of the input reference signal. During the time period **A**, if the phase and frequency of the output timing signal F_{out} and input reference signal F_{ref} are aligned, the signal **UP** and the signal **DOWN** have an equal pulse width. As shown during time period **B**, if the phase of the output timing signal F_{out} lags or the frequency is lower than the input reference signal F_{ref}, the signal **UP** has a pulse width longer than the signal **DOWN**. If the phase of the output timing signal F_{out} leads or the frequency is higher than the input reference signal F_{ref}, the signal **DOWN** has a pulse width longer than the signal **UP**. The charge pump **15** responds appropriately to create the necessary current I_{CP}, which, when filtered, creates the input voltage V_{IN} to adjust the voltage controlled oscillator **25**.

[0009] Determination of phase-frequency lock of the phase lock loop **5** is important for the functioning of circuits that are to receive and extract the data from the transport signal. Generally, the circuits provide lock notification signals indicating that the phase lock loop is in phase-

frequency synchronization. U.S. Patent 6,215,834 (McCollough), U. S. Patent 5,886,582 (Stansell), U. S. Patent 5,870,002 (Ghaderi et al.), U. S. Patent 5,838,749 (Casper et al.), U. S. Patent 5,822,387 (Mar), U. S. Patent 5,724,007 (Mar), and U. S. Patent 5,394,444 (Silvey et al.) are illustrative of circuits and systems that provide such notification of the phase-frequency synchronization. These notification signals provide only an indication of phase-frequency synchronization and do not indicate a loss of phase-frequency synchronization. However, U. S. Patent 4,499,434 (Thompson) does provide an alarm indicating loss of the phase-frequency synchronization.

Summary of the Invention

[0010] An object of this invention is to provide a circuit that determines whether an output signal of a phase lock loop is in phase-frequency synchronization with an input reference timing signal.

[0011] Another object of this invention is to provide a circuit that generates an unlock alarm signal indicating that an output signal of a phase lock loop is no longer in phase-frequency synchronization with an input reference timing signal.

[0012] To accomplish at least one of these and other objects, a lock detection circuit that is in communication with the phase lock loop has a first logic function circuit to combine a frequency increase signal and a

frequency decrease signal of the phase lock loop to provide a frequency deviation signal. The first logic function in the preferred embodiment of this invention is an OR gate. The output of the first logic function circuit is an input to a second logic function circuit. The second logic function circuit combines the frequency deviation signal with the input reference signal, which is applied to a second input of the second logic function, to determine that the frequency deviation signal has a greater duration than a desired portion of a cycle of the input reference signal and provide an unlock alarm signal. The desired portion of a cycle of the input reference signal is proportionally related to the level of jitter tolerated between the input reference signal and the output timing signal. The second logic function circuit in the preferred embodiment of this invention is an AND gate.

[0013] The lock detection circuit further includes a latching circuit in communication with the second logic function and the input reference signal to capture and retain the unlock alarm signal indicating loss of phase-frequency lock of the phase lock loop. The unlock alarm signal is transferred to external circuitry such that the external circuit is alerted that data received from a network connection is no longer synchronized and may be corrupted.

[0014] In a second embodiment of the lock detection circuit, an integrator circuit replaces the latching circuit. The integrator circuit is in

communication with the second logic function to receive and integrate the error signal. Upon the integrated error signal achieving an integrated threshold level, an unlock alarm is generated to indicate loss of phase-frequency lock of the phase lock loop.

[0015] In a third embodiment, the lock detection circuit further includes a frequency divider. The frequency divider is connected to receive the input reference signal, divide the input reference signal, and transfer the divided input reference signal to the second function circuit. The second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

[0016] An alternate embodiment of the lock detection circuit of this invention includes a phase-frequency detector. The phase-frequency detector is in communication with the phase lock loop to receive the output frequency signal and the input reference signal to generate a frequency increase signal and a frequency decrease signal. The frequency increase signal and the frequency decrease signal are indicative of an amount of phase-frequency deviation of the output frequency signal has from the input reference signal. The output of the phase frequency detector is applied to a first logic function circuit. The first logic function in this embodiment combines the frequency increase signal and the frequency decrease signal to provide a frequency deviation signal. The frequency deviation signal is combined with the input reference signal in a second

logic function circuit to determine the frequency deviation signal. If the frequency deviation signal has a greater duration than the desired portion of a cycle of the input reference signal, the second logic function circuit provides the error signal.

Brief Description of the Drawings

[0017] Fig. 1 is a functional block diagram of phase lock loop of the prior art.

[0018] Fig. 2 is plot of the outputs of the phase-frequency detector and the input reference signal of Fig. 1.

[0019] Figs. 2a and 3b are plots of input signals and the unlock alarm signal of the lock detector circuit of this invention.

[0020] Fig. 4 is functional block diagram of a phase lock loop with an unlock detector of this invention.

[0021] Fig. 5 is a logic diagram of a first embodiment of the lock detector circuit of this invention.

[0022] Fig. 5 is a logic diagram of a second embodiment of the lock detector circuit of this invention.

[0023] Fig. 7 is a logic diagram of a third embodiment of the lock detector circuit of this invention.

[0024] Fig. 8 is functional block diagram of an alternate embodiment of a phase lock loop with an unlock detector of this invention.

[0025] Fig. 9 is a logic diagram of a fourth embodiment of the lock detector circuit of this invention.

Detailed Description of the Invention

[0026] As shown in Fig. 2, the output signals **UP** and **DOWN** of the phase frequency detector provides an indication of the deviation or jitter of the phase-frequency of the output timing signal $\mathbf{F_{out}}$ of the voltage control oscillator from the input reference frequency signal $\mathbf{F_{ref}}$. If the duration of the output signals **UP** or **DOWN** become too great, the output timing signal $\mathbf{F_{out}}$ is said to no longer locked with the input reference frequency signal $\mathbf{F_{ref}}$. The length of the duration of the output signals **UP** and **DOWN** that is allowable is a function of the level of the jitter that exists between the output timing signal $\mathbf{F_{out}}$ and the input reference signal $\mathbf{F_{ref}}$. Since there is no inherent signal within a phase lock loop to alert for excessive jitter or phase-frequency unlock, a circuit needs to added to the phase lock loop to provide the alarm of an unlock.

[0027] This alarm is used in telecommunication systems such a SONET to provide an alert to a receiver indicating the timing signal is not accurately recovered and the in coming data is corrupted. The SONET system then

has extensive error correction and recovery techniques to insure accurate transfer of the communication signals.

[0028] Referring now to Figs. 3a and 3b for a discussion of lock detection in a phase lock loop of this invention. In Fig. 3a, the phase-frequency deviation is determined at the time t_X and the **UP** signal is shown to extend longer than one-half cycle of the input reference signal F_{ref}. This indicates that the phase error of the output timing signal F_{out} leads or has a higher frequency than the input reference signal F_{ref}. Alternately, in Fig. 3b, the phase-frequency deviation is determined at the time t_X and the **DOWN** signal is shown to extend longer than one-half cycle of the input reference signal F_{ref}. This indicates that the phase error of the output timing signal F_{out} lags or has a lower frequency than the input reference signal F_{ref}. If the amount of jitter or deviation of output timing signal F_{out} causes the deviation signals **UP** or **DOWN** to extend beyond the time t_Y, the phase lock loop is considered to be no longer locked and, as described above, any received data is now corrupted. In a phase lock loop incorporating a lock detection circuit of this invention, an unlock alarm signal $\overline{\textbf{LOCK}}$ becomes active when either the **UP** or **DOWN** deviation signals extend greater than the time t_Y. The time t_Y in this example is exactly one-half cycle of the input reference signal F_{ref}. However, as will be shown in subsequent embodiments the timing of the unlock alarm signal $\overline{\textbf{LOCK}}$ can be adjusted to account for differences in frequency deviation or jitter that can be tolerated in a communication system.

[0029] Fig. 4 illustrates a first embodiment of a phase lock loop incorporating a lock detection circuit **100** of this invention. The structure and operation of the basic phase components of the phase lock loop **5** are as described for Fig. 1. The output of the phase-frequency detector **UP** and **DOWN** and the input reference signal F_{ref} are the inputs to the lock detection circuit **100**. The lock detection circuit **100** logically combines the output signals **UP** and **DOWN** to determine the amount of deviation that the output timing signal F_{out} has versus the input reference signal F_{ref}. The amount of deviation is compared to the input reference signal F_{ref} and as shown in Figs 3a and 3b, if the deviation is greater than one-half cycle of the input reference signal F_{ref}, the unlock alarm signal $\overline{\textbf{LOCK}}$ is set or latched at the time t_Y.

[0030] Refer now to Fig. 5 for a discussion of the structure and operation of the lock detection circuit **100**. The output signals **Up** and **DOWN** of the phase-frequency detector **10** of Fig. 4 are logically combined in the OR gate **105** to form the deviation signal **DEV**. The deviation signal **DEV** and the input reference signal are logically combined by the AND gate **110** to form the error signal **ERR**. The error signal **ERR**, as shown in Figs. 3a and 3b, becomes active at the time t_Y and has a duration of from the time t_Y to the time t_Z.

[0031] Ideally the error signal **ERR** would have sufficient duration to be interpreted by external circuitry as the unlock alarm signal $\overline{\textbf{LOCK}}$.

However, in many instances, the duration of the error signal **ERR** maybe insufficient to be transferred for use by external circuitry of a communication system. To insure capture of the error signal **ERR** the lock detection circuit may optionally include a latch or flip-flop **FF1 115**. The error signal **ERR** is the set input of the latch **115** and the input reference signal $\mathbf{F_{ref}}$ is the clock input of the latch **115**. As shown in Figs. 3a and 3b, at the rising edge of the input reference signal $\mathbf{F_{ref}}$, the latch **115** captures and retains the error signal **ERR** to create the unlock alarm signal $\overline{\mathbf{LOCK}}$. The latch is intended to be provided by the external circuitry as part of the recognition of the loss of lock condition, therefore reset for the latch **115** is provided by the external circuitry.

[0032] A second embodiment of the lock detection circuit of this invention is shown in Fig. 6. In this embodiment the latch **115** of Fig. 5 is substituted with an integrator **125**. The integrator **125** receives the error signal **ERR** and integrates the signal to form the unlock alarm signal $\overline{\mathbf{LOCK}}$. In this instance the integrator **125** is structured such that the energy present in the error signal **ERR** determines the output level of the unlock alarm signal $\overline{\mathbf{LOCK}}$. The integrator is designed such that the deviation or jitter of the output timing signal $\mathbf{F_{out}}$ versus the input reference signal $\mathbf{F_{ref}}$ is set to any desired amount of deviation or jitter.

[0033] The integrator **125** has differential amplifier **130**, a resistor **135**, and a capacitor **140**. The structure and operation is well known in the art and

will not be discussed further. The output voltage of the differential amplifier **130** is the unlock alarm signal $\overline{\textbf{LOCK}}$ and is equal to

$$V_{unlck} = \frac{1}{RC}\int V_{err}dt$$

where:

V_{unlck} is the magnitude as a function of time of the unlock alarm signal $\overline{\textbf{LOCK}}$.

V_{ERR} is the magnitude as a function of time of the error signal **ERR**.

R is the resistance of the resistor **135**.

C is the capacitance of the capacitor **140**.

[0034] In this embodiment the unlock alarm signal $\overline{\textbf{LOCK}}$ is received by a Schmidt trigger or comparator to assure appropriate logic level for the external circuitry. In practical terms, the unlock alarm signal $\overline{\textbf{LOCK}}$ is transferred to a latch or D-type flip-flop with an external reset that has sufficient hysterisis to trigger the unlock alarm signal $\overline{\textbf{LOCK}}$ correctly.

[0035] Fig. 7 is an illustration of a third embodiment of the lock detection circuit incorporated in the phase lock loop of this invention. In this instance the lock detection circuit is structured and operates as described

in Fig. 5 except in this instance the level of jitter is greater than the one-half cycle as shown in Fig. 5. To accomplish this the input reference frequency $\mathbf{F_{ref}}$ is applied to a frequency divider **145**. The output of the frequency divider **145** is now the input to the AND gate **110** to be combined with the deviation signal **DEV** to form the error signal **ERR**. As described for the error signal **ERR** of Fig. 5, the error signal **ERR** may be transferred directly to the external circuitry. However, it is likely that the duration of the error signal **ERR** may be insufficient for use by the external circuitry and must be captured and retained as described above in the latch **115**.

[0036] It would be obvious to one skilled in the art that the integrator **125** of Fig. 6 could be substituted for the latch **115** and still be in keeping with the intent of this invention. The integrator would function as described for Fig. 6 except the timing would be determined by the divided input reference frequency signal **147**.

[0037] Referring now to Fig. 8 for a discussion of a fourth embodiment of the lock detection circuit incorporated in a phase lock loop of this invention. The phase lock loop **5** is structure and functions as described for Fig. 1. The lock detection circuit **200** in this embodiment has the output timing signal $\mathbf{F_{out}}$ and the input reference signal $\mathbf{F_{ref}}$ as inputs. The phase-frequency deviation is directly determined and the unlock alarm signal $\overline{\mathbf{LOCK}}$ is activated when the phase-frequency deviation between

the output timing signal F_{out} and the input reference signal F_{ref} is greater than an amount allowed for application of the phase lock loop.

[0038] The lock detection circuit **200**, as shown in Fig. 9 is fundamentally as structure in Fig. 5, except in this embodiment, the output timing signal F_{out} is an input to the frequency divider circuit **225**. The input reference signal F_{ref} and the frequency divided signal from the frequency divider circuit 225 are applied to a separate phase-frequency detector **205**. The separate phase-frequency detector **205** functions at a different frequency than the phase–frequency detector **10** of Fig. 8. The proportionality of the duration of the deviation output signals **UP 2** and **DOWN 2** of the phase-frequency detector **205** versus the input reference signal F_{ref} is used to determine the amount of deviation or jitter that the phase lock loop can accept before activating the unlock alarm signal $\overline{\textbf{LOCK}}$. The deviation output signals **UP 2** and **DOWN 2** are logically combined in the OR gate **210** to form the deviation signal **DEV**. The deviation signal **DEV** and the input reference signal F_{ref} are logically combined in the AND gate **215** to form the error signal **ERR**. The error signal **ERR** may be transferred to external circuitry or may be captured and retained in the latch **220** as described above.

[0039] As is known in the art, the function of a phase lock loop maybe accomplished as a process within a computation device such as a microcomputer, microcontroller, or digital signal processor. Similarly, the

lock detection circuit of this invention can be accomplished as a process within the process of the phase lock loop.

[0040] The method for providing an unlock alarm that denotes loss of phase frequency synchronism of a phase lock loop begins by providing an increase frequency signal and a decrease frequency signal from the phase lock loop generation process. The increase and decrease frequency signals indicate existence of an error in the phase-frequency between an input reference timing signal to the phase lock loop and an output local oscillator signal. A first logical combining of the increase frequency signal and the decrease frequency signal is performed to create a phase-frequency deviation signal. In the preferred embodiment of this method, this first logical combining is an ORing of increase and decrease frequency signals. A second logical combining of the phase-frequency deviation signal and the input reference timing signal is then performed. In the preferred embodiment of this invention, the second logical combining is an ANDing of the phase-frequency deviation signal and the input reference timing signal. If the phase-frequency deviation signal has a greater duration than a portion of a cycle of the timing signal, the unlock alarm signal is provided. Since the duration of the unlock alarm signal maybe small, the method may include a capturing and retaining of the unlock alarm signal for transfer to external circuitry.

[0041] An alternate to the capturing and retaining the unlock alarm signal is executed in a second embodiment of the method of this invention by integrating the unlock alarm signal. A threshold at which the unlock alarm signal is deemed to be critical to the reception of incoming data is set and the unlock alarm signal is then transferred to an external process for recovery of any lost data.

[0042] A third embodiment of the method of this invention divides the frequency of the input reference signal by a factor sufficient to establish the level of jitter or phase-frequency difference to be tolerated by the communication system. Subsequent to the dividing of the input reference signal the second logical combining of the deviation signal now occurs with the divided input reference signal. While the dividing factor for the input reference signal maybe any real number, for practical purposes the factor is an integer that adjusts the rising edge relative of the divided input reference signal relative to the allowable jitter.

[0043] In a fourth embodiment of the method of this invention, the increase and decrease frequency signals are derived independently from the input reference signal and the output timing signal of the phase lock loop. The derivation is a result of the comparison of the phase-frequency of the output timing signal to the input reference signal and providing an indication of phase lead of the output timing signal and the input reference signal (greater frequency) or of phase lag (lower frequency). The extent of

the difference in the output timing signal and the input reference signal are shown as the magnitude and duration of the increase and decrease frequency signals and are adjusted by improving the sensitivity of the comparison of the phase-frequency of the output timing signal with the input reference signal.

[0044] While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

[0045] The invention claimed is: